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SEMICONDUCTOR INTEGRATED CIRCUIT

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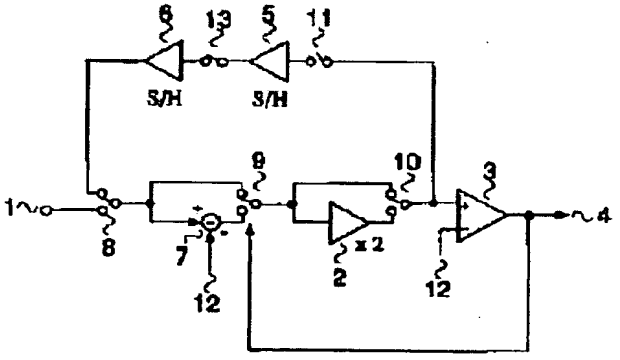
Abstract of **JP11027148**

PROBLEM TO BE SOLVED: To prevent the increase of a circuit scale and the increase of power consumption from being invited even if a D/A converter is used. SOLUTION: This circuit has signal amplifying means (2 and 10) which switch gain to one time or two times, operation processing means (7 and 9) which perform subtraction processing of a signal to be inputted and reference voltage and output them or output them without performing subtraction processing, a switching means 8 in which one switch terminal is connected to a signal input terminal, the other switch terminal is also connected to output sides of sample-and-hold means (5 and 6) and a common terminal is connected to an input side of the operation processing means, a comparator 3 which compares an output of the signal amplifying means with reference voltage and binarizes it and a switching means 11 which connects an output side of the signal amplifying means and an input side of the sample hold means. Here, the operation processing means switches between performing subtraction processing of a signal to be inputted and reference voltage to output and outputting them without performing subtraction processing based on an



output of the comparator 3.

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BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor integrated circuit and a driving method thereof and, more particularly, to a semiconductor integrated circuit suitably applicable to a successive comparison A-D converter, and a driving method thereof.

2. Related Background Art

With present development of digital signal processing, the A-D converters for converting an analog signal to a digital signal are important technology and the A-D converters of various methods (hereinafter referred to as AD converters) have been developed heretofore. Particularly in high-speed applications, the mainstream converters are flash AD converters wherein there are comparison voltages corresponding to all levels of a quantization range and in the case of N-bit conversion, the converter has (2N-1) comparators for concurrent comparison and encoding. Since the number of comparators was large, such AD converters were not suitable for applications to portable remote terminals and the like requiring low power consumption. Therefore, the successive comparison AD converters, which are AD converters of low power consumption, have widely been and are used.

FIG. 1 is a block diagram to show an example of the successive comparison AD converter. An analog signal to be converted is applied to input terminal 50 to be input to a (+) input terminal of comparator 51. Connected to a (-) input terminal of the comparator 51 is an output of D-A converter 54 whose input bit is set by successive comparison register 53 and which generates a comparison analog voltage.

A control circuit 52 sets a value of the successive comparison control register 53, based on a result of the comparator 51, to control the output of the DA converter 54. In the successive comparison AD converter, the analog signal input is successively converted bit by bit from MSB (Most Significant Bit) into a digital code. Let us consider successive comparison of N bits. In response to a control signal from the control circuit 52, the successive comparison register sets 1 at the N-th bit, which is the MSB, and 0 to the other bits. This code is applied to the DA converter 54 to be converted into an analog comparison signal Vda. In this case, the analog comparison signal Vda is generated as a voltage equal to a half of the entire quantization range, which is compared with the analog input signal Vin applied to the input terminal 50. When Vin>Vda, the output from the comparator 51 becomes "H" to be sent to the control circuit 52. Receiving "H", the control circuit 52 rewrites the data in the successive comparison register so as to set 1 to the lower bit (MSB-1) while maintaining 1 in the MSB, which is the bit having been compared so far, and then sends the result to the DA converter 54. In this case, the MSB bit is determined to be 1 and the next comparison operation is carried out with setting 1 in the (MSB-1) bit. When Vin<Vda, the output of the comparator 51 is "L" and is sent to the control circuit 52. Receiving "L", the control circuit 52 rewrites the data in the successive comparison register so as to change the MSB, which is the bit having been compared so far, from 1 to 0 and set 1 in the lower bit (MSB-1), and sends the result to the DA converter 54. In this case, the MSB bit is determined to be 0, and then the next comparison operation is carried out

with setting 1 in the (MSB-1) bit. This operation is repeated while performing the comparison and register setting in order from the upper bit to the lower bit, so that the data of the successive comparison register finally becomes a binary code resulting from the A-D conversion of the analog input signal Vin applied to the input terminal 50.

For configuring a successive comparison AD converter with many bits, however, the successive comparison AD converter shown in FIG. 1 was not suitable because the number of bits of the DA converter 54 for generating the analog comparison voltage needed to be the same as the number of bits of the AD converter, resulting in increasing the circuit scale and in turn increasing power consumption. The conversion accuracy of the AD converter of the successive conversion method was mainly dependent upon errors of the DA converter 54, and the increase in the number of bits degraded the accuracy of DA converter 54. As a result, the AD convertor came to lack monotonicity and make a coding error.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a semiconductor integrated circuit that can perform highly accurate A-D conversion by a simple circuit configuration, and a driving method thereof.

Another object of the present invention is to provide a semiconductor integrated circuit that can perform the A-D conversion operation with low power consumption and in high integration without increase in the circuit scale, and a driving method thereof.

Still another object of the present invention is to provide a semiconductor integrated circuit comprising: signal amplifying means (2, 10 in FIG. 2) capable of switching a gain, preferably, to 1 or 2; arithmetic processing means (7, 9 in FIG. 2) connected to an input side of the signal amplifying means, the arithmetic processing means carrying out a subtraction process of a reference voltage from a signal input thereto to output a result of the subtraction process, or outputting the signal input thereto without performing the subtraction process; changeover means (8 in FIG. 2) whose one changeover terminal is connected to a signal input terminal (1 in FIG. 2) and whose other changeover terminal is connected to an output side of sample hold means (5, 6 in FIG. 2), a common terminal of the changeover means being connected to an input side of the arithmetic processing means; a comparator (3 in FIG. 2) connected to an output side of the signal amplifying means, the comparator comparing an output from the signal amplifying means with the reference voltage (12 in FIG. 2) to binarize the output; and switch means (11 in FIG. 2) connecting the output side of the signal amplifying means to an input side of the sample hold means;

wherein the arithmetic processing means (7, 9 in FIG. 2) carries out a changeover (a changeover of 9 in FIG. 2) between performing the subtraction process of the reference voltage from the signal input thereto to output the result and outputting the signal input without performing the subtraction process, based on an output from the comparator (3 in FIG. 2).

Another object of the present invention is to provide a semiconductor integrated circuit comprising: signal amplifying means (2 in FIG. 4) capable of switching a gain, preferably, to 1 or 2 and capable of performing a changeover between performing a subtraction process of a reference voltage from a signal input thereto to output a result of the subtraction process and outputting the signal input thereto without performing the subtraction process; changeover means (8 in FIG. 4) whose one changeover terminal is connected to a signal input terminal (1 in FIG. 4) and whose other changeover terminal is connected to an output side of sample hold means (5, 6 in FIG. 4), a common terminal of the changeover means being connected to an input side of the signal amplifying means; a comparator (3 in FIG. 4) connected to an output side of the signal amplifying means, the comparator comparing an output from the signal amplifying means with the reference voltage (12 in FIG. 4) to binarize the output; and switch means (11 in FIG. 4) connecting the output side of the signal amplifying means to an input side of the sample hold means; wherein the signal

amplifying means (2 in FIG. 4) carries out the changeover (a changeover of 9 in FIG. 4) between performing the subtraction process of the reference voltage from the signal input thereto to output the result and outputting the signal input thereto without performing the subtraction process, based on an output from the comparator (3 in FIG. 4).

Still another object of the present invention is to provide a method for driving a semiconductor integrated circuit comprising: signal amplifying means capable of switching a gain; arithmetic processing means connected to an input side of the signal amplifying means, the arithmetic processing means carrying out a subtraction process of a reference voltage from a signal input thereto to output a result of the subtraction process, or outputting the signal input thereto without performing the substraction process; changeover means whose one changeover terminal is connected to a signal input terminal and whose other changeover terminal is connected to an output side of sample hold means, a common terminal of the changeover means being connected to an input side of the arithmetic processing means; a comparator connected to an output side of the signal amplifying means, the comparator comparing an output from the signal amplifying means with the reference voltage to binarize the output; and switch means connecting the output side of the signal amplifying means to an input side of the sample hold means; wherein the arithmetic processing means carries out a changeover between performing the subtraction process of the reference voltage from the signal input thereto to output the result and outputting the signal input thereto without performing the subtraction process, based on an output from the comparator, the driving method comprising an MSB (Most Significant Bit) conversion mode in which the gain of the signal amplifying means is set to 1 and the changeover means electrically connects the signal input terminal to the input side of the arithmetic processing means.

A further object of the present invention is to provide a method for driving a semiconductor integrated circuit comprising: signal amplifying means capable of switching a gain and capable of performing a changeover between performing a subtraction process of a reference voltage from a signal input thereto to output a result of the subtraction process and outputting the signal input thereto without performing the subtraction process; changeover means whose one changeover terminal is connected to a signal input terminal and whose other changeover terminal is connected to an output side of sample hold means, a common terminal of the changeover means being connected to an input side of the signal amplifying means; a comparator connected to an output side of the signal amplifying means, the comparator comparing an output from the signal amplifying means with the reference voltage to binarize the output; and switch means connecting the output side of the signal amplifying means to an input side of the sample hold means; wherein the signal amplifying means carries out the changeover between performing the subtraction process of the reference voltage from the signal input thereto to output the result and outputting the signal input thereto without performing the subtraction process, based on an output from the comparator, the driving method comprising an MSB (Most Significant Bit) conversion mode in which the gain of the signal amplifying means is set to 1 and the changeover means electrically connects the signal input terminal to the input side of the signal amplifying means.

The present invention can realize the successive conversion operation by comparing an input analog signal with the reference voltage 12 of the reference power supply and feeding the input analog signal as it is or a difference resulting from the subtraction of the reference voltage value therefrom back to the input, based on the comparison result; therefore, the present invention can achieve the simple circuit of low power consumption using only the comparator but necessitating no DA converter. This permits the highly accurate successive conversion AD converter to be constructed without increase in hardware against increase in the number of conversion bits.

In a preferred embodiment of the present invention, the gain of the signal amplifying means 2 is set to 1 in the MSB conversion mode where the first changeover means 8 electrically connects the signal input terminal 1 to the input side of the arithmetic processing means (7, 9 in FIG. 2) or the signal amplifying

means (2 in FIG. 4), or the gain of the signal amplifying means 2 is set to 2 in the conversion mode except for the MSB conversion mode, where the first changeover means electrically connects the signal input terminal to the output side of the sample hold circuit.

This setup realizes the successive comparison AD converter with the reduced number of circuit elements, which can be set in each bit conversion mode simply by switching the gain of the signal amplifying means between in the MSB conversion mode and in the conversion mode except for the MSB conversion mode.

In a preferred embodiment of the present invention, after such an operation that a signal before AD conversion is applied to the signal input terminal 1, that the signal is amplified by a factor of 1 or 2 by the signal amplifying means 2, and that a binary comparison operation of the comparator 3 is completed, first switch means 11 is switched on, whereby either after execution of the subtraction process of subtracting a signal of the reference voltage from the signal before the AD conversion when the output of the comparator is active or after execution of an arithmetic process of not performing the subtraction process of the signal of the reference voltage from the signal before the AD conversion when the output of the comparator is non-active, an output from the signal amplifying means is supplied to the sample hold circuit 5.

This setup achieves highly accurate AD conversion even with increase in the number of conversion bits using only a 1-bit AD converter in terms of the hardware in such a way that the suitable processes are carried out for the input analog signal to be converted, based on the quantized result, by use of one comparator or 1-bit AD converter and the signal is held as input information of the next conversion bit.

In a preferred embodiment of the present invention, the signal amplifying means comprises an operational amplifier (2 in FIG. 4), a non-inverting input terminal of the operational amplifier is connected through first capacitor means (23 in FIG. 4) to second changeover means (20 in FIG. 4), one terminal of the second changeover means is connected to a second reference power supply (27 in FIG. 4), the other terminal is connected to an output of the first changeover means (8 in FIG. 4), an inverting input terminal of the operational amplifier is connected through second capacitor means (24 in FIG. 4) to third changeover means (9 in FIG. 4) and also connected through third capacitor means (25 in FIG. 4) to the output of the operational amplifier, one terminal of the third changeover means is connected to the ground potential (27 in FIG. 4), the other terminal is connected to the first reference power supply (12 in FIG. 4), and the third changeover means is controlled by a binary output from the comparator.

This setup permits the difference between the input voltage value and the reference voltage value to be input accurately by alternate writing of the reference voltage value and the input signal value through the first capacitor means connected to the non-inverting input terminal of the operational amplifier, thus realizing the accurate signal processing without being affected by the offset of the operational amplifier or the like. Since the conversion operation of the compared input analog signal to the lower bit can be realized by the simple control and circuit configuration wherein the circuit has the switch (changeover means) connected through the second capacitor means connected to the inverting terminal of the operational amplifier to the ground potential or to the reference voltage value and wherein the switch is flipped to the reference voltage value in the reset mode or either to the reference voltage value or to the ground potential after the AD conversion, based on the output result of the comparator or 1-bit AD converter, the accuracy of range conversion can be improved remarkably and the number of quantization conversion bits of the successive comparison AD converter can be increased greatly.

In a preferred embodiment of the present invention, the third changeover means (9 in FIG. 4) is connected to the first reference power supply (12 in FIG. 4) when the binary output of the comparator (3 in FIG. 4) is active; whereas the third changeover means is connected to the ground potential (27 in FIG. 4) when the binary output is non-active.

In this setup, according to the bit conversion result, with the bit output of "H" the voltage equal to a half of the full range is subtracted from the input analog signal and the result is returned to the feedback loop; with the bit output of "L" the input analog signal is returned to the feedback loop without any process, whereby only one stage of the capacitance-coupled operational amplifier can perform the subtraction process etc. necessary for comparison of the next bit output, which enhances the accuracy, which realizes the processing circuit without a need for a special circuit, and which decreases the power consumption.

As described above, the present invention employs the signal loop circuit configuration using the capacitance-coupled operational amplifier, sample hold circuits, and 1-bit quantizing comparator to perform the quantization judgment in order from the MSB of the upper bit, thereafter perform the subtraction process from the input analog signal, based on the quantization result, perform the range expanding process, and feed the analog signal after these processes back to the input, and then perform the quantization operation of the next bit, whereby the analog processing can be carried out with high accuracy by the simple configuration including the one-stage capacitance-coupled operational amplifier and sample hold circuits, thereby realizing the successive comparison AD converter for a string of many bits in the small circuit scale, in high integration, and with low power consumption while drastically improving the quantization conversion error.

The configurations according to the present invention were described above referring to FIG. 2 and FIG. 4, but it should be noted that the present invention is by no means intended to be limited to only the configurations of FIG. 2 and FIG. 4 nor to the embodiments described hereinafter. A variety of modifications and combinations can also be suitably contemplated according to the necessity within the spirit and scope of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic circuit diagram for explaining an example of the successive comparison AD converter;

FIG. 2 is a schematic circuit diagram for explaining an example of the semiconductor integrated circuit according to the present invention;

FIG. 3 is a drawing for explaining an example of the operation in the circuit shown in FIG. 2;

FIG. 4 is a schematic circuit diagram for explaining another example of the semiconductor integrated circuit according to the present invention;

FIGS. 5, 6, 7 and 8 are circuit diagrams for explaining an example of the operation in the circuit shown in FIG. 4; and

FIGS. 9, 10, 11 and 12 are circuit diagrams for explaining an example of the operation in the circuit shown in FIG. 4 after the MSB (Most Significant Bit).

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The embodiments of the present invention will be described in detail by reference to the drawings.

First Embodiment

FIG. 2 is a schematic circuit diagram t o show the first embodiment of the present invention. In FIG. 2, an analog signal to undergo the A-D conversion is applied to the input terminal 1 to be input through switches

8, 9, 10 to a non-inverting input terminal (+input terminal) of comparator 3. A reference voltage is applied from a reference power supply 12 to an inverting input terminal (-input terminal) of the comparator 3. When the analog signal applied to the input terminal 1 is larger than the reference voltage of the reference power supply 12, the output of the comparator 3 becomes "H"; when smaller, the output of the comparator 3 becomes "L". The reference power supply 12 is a dc voltage source having a voltage value (Vref) equal to a half of a voltage full range Vfull which the analog signal to undergo the AD conversion can take. Namely, the relation of Vref=Vfull/2 exists. Since the successive comparison AD converter in the present embodiment performs the AD conversion successively from the most significant bit MSB, the operation in the above description is the one in a mode upon conversion of MSB. When the analog signal applied to the input terminal 1 is larger than the reference voltage of the reference power supply 12 and thus the output of the comparator 3 is "H", a quantizing value of MSB is determined to be 1 and the switch 9 is controlled so that an output of the switch 9 is an output of a subtractor 7 for subtracting the reference voltage value of the reference power supply 12 from the analog signal applied to the input terminal 1.

As a preparation operation for AD conversion of a lower bit, the signal passes through signal amplifier 2 for doubling the analog signal having undergone subtraction, so as to be amplified twice and expand the range. The amplified signal becomes an output of the switch 10. When the analog signal applied to the input terminal 1 is smaller than the reference voltage of the reference power supply 12 and thus the output of the comparator 3 is "L", a quantizing value of MSB is determined to be 0 and the switch 9 is controlled so that the analog signal applied to the input terminal 1 is outputted as an output of the switch 9 as it is. As a preparation operation for AD conversion of a lower bit, the signal then passes through the signal amplifier 2 for doubling the analog signal being the output of the switch 9, so as to be amplified twice and expand the range. The amplified signal is outputted as an output of the switch 10. The analog signal thus processed for conversion of the lower bit is supplied through switch 11 to a first sample hold circuit (S/H) 5 to be held there temporarily. After completion of the quantization operation in the AD conversion section, the switch 11 is switched off and switch 13 is switched on whereby the analog signal for AD conversion of the next bit is input into a second sample hold circuit (S/H) 6. Then the switch 13 is switched off to hold this value. Then the switch 8 turns into a mode for supplying an output of the sample hold circuit 6 to the AD conversion section. In the processes of the other bits than the MSB, the output of the sample hold circuit 6 is set to be an output of switch 8. Namely, in the processes of the other bits than the MSB the output signal of the AD conversion section is fed through the sample hold circuits 5, 6 back to the input of the AD conversion section.

FIG. 3 is a drawing for explaining the AD conversion architecture of the present embodiment. The illustration of FIG. 3 is an example where the successive comparison AD converter is of three bits in the present embodiment, but it is a matter of course that the AD converters according to the present invention are not limited to this number of bits.

The analog signal applied to the input terminal 1 in FIG. 2 is indicated by 14 in FIG. 3. Numeral 119 designates the quantization range of the input analog signal in the MSB, and the quantization range is equally divided into three bits, i.e., into eight levels. Quantization representative points 000 to 111 are assigned to the respective quantization levels. The reference potential, Vref, of the reference power supply 12 in the comparator of FIG. 2 is located at the center of the quantization range 119. When the signal surpasses this value, the output of the comparator 3 of FIG. 2 becomes "H" whereby the quantization code of the MSB is determined to be "1". When the input analog signal does not surpass this value, the output of the comparator 3 becomes "L" and the quantization code of the MSB is determined to be "0". In the example of FIG. 3, because the input analog signal 14 is smaller than the reference potential Vref 12, the output of the comparator (Comp) 3 becomes "L" and the MSB is determined to be "0".

For next carrying out quantization of the (MSB1) bit being the next lower bit, the signal is supplied to the signal amplifier 2 having the gain of 2 without passing the subtractor 7 of FIG. 2, because the analog signal

in the MSB was smaller than the reference potential Vref 12 and thus the output of the comparator 3 was "L". The signal undergoes analog amplification by the signal amplifier 2 to expand the range twice, thus becoming the analog signal indicated by 15 in FIG. 3. This signal is fed through the sample hold circuits 5, 6 of FIG. 2 back to the input of the AD conversion section to undergo the AD conversion of the (MSB-1) bit. Since the signal this time is the one after expansion of the range, the quantization range 120 for the analog signal 15 of FIG. 3 input into the AD conversion section is double the levels below the reference potential Vref 12 of the quantization range 119 for the MSB, whereby quantization of the (MSB-1) bit is realized. Since the quantization range 120 is expanded to double the quantization range 119, the quantization range has the quantization levels obtained by quartering the full range. The reference potential Vref 12 of the reference power supply at the comparator 3 of FIG. 2 is located at the center of the quantization range 120. When the signal surpasses this value, the output of the comparator 3 of FIG. 2 becomes "H" and the quantization code of (MSB-1) is determined to be "1". When the input analog signal is smaller than this value, the output of the comparator 3 becomes "L" and the quantization code of (MSB-1) is determined to be "0". Since in the example of FIG. 3 the input analog signal 15 is larger than the reference potential Vref 12, the output of the comparator 3 is "H" and (MSB-1) is determined to be "1".

For next quantizing the (MSB-2) bit being the next lower bit, because the analog signal 15 in the (MSB-1) was over the reference potential Vref 12 and thus the output of the comparator 3 was "H", an analog signal 17, resulting from subtraction of a portion of the analog signal 15 corresponding to the reference potential Vref 12 from the analog signal 15 input to the subtractor 7 of FIG. 2, undergoes analog amplification by the signal amplifier 2 having the gain of 2, so as to double the range, thus becoming an analog signal 18 shown in FIG. 3. Then the analog signal 18 is fed through the sample hold circuits 5, 6 of FIG. 2 back to the input of the AD conversion section to undergo the AD conversion for the bit of MSB-2 (LSB). Since the signal at this time is the one after expansion of the range, the quantization range 121 for the analog signal 18 of FIG. 3 input to the AD conversion section is double the levels above the reference potential Vref 12 of the quantization range 120 for the (MSB-1), thus realizing the range expanding operation for quantization of the (MSB-2) bit. Since the quantization range 121 is twice larger than the quantization range 120, the quantization range 121 has quantization levels obtained by halving the full range, and the reference potential Vref 12 of the reference power supply at the comparator 3 in FIG. 2 is located at the center of the quantization range 121. When the signal surpasses this value, the output of the comparator 3 of FIG. 2 becomes "H", so that the quantization code of MSB-2 (LSB) is determined to be "1". When the input analog signal is smaller than this value, the output of the comparator 3 becomes "L" and the quantization code of MSB-2 (LSB) is determined to be "0". In the example of FIG. 3 where the input analog signal 18 is larger than the reference potential Vref 12, the output of the comparator 3 is "H" and MSB-2 (LSB) is determined to be "1". This completes the successive comparison of MSB, MSB-1, and MSB-2 (LSB) to encode the input signal to the AD conversion code of 011.

As described above, it becomes possible to perform highly accurate successive comparison by such a simple circuit configuration as to expand the range of the analog signal after the AD conversion, feed the range-expanded signal back to the AD conversion section by the feedback loop, and again subject the signal to the AD conversion. Accordingly, the DA converter 54 shown in FIG. 1 is not necessary; and with increase in the number of quantizing bits of the AD conversion, to achieve high accuracy was difficult by the circuit configuration of FIG. 1 because the accuracy of the AD conversion was determined by the conversion accuracy of the internal DA converter 54; whereas the present embodiment is arranged so that the accuracy of the AD conversion is determined only by the subtraction accuracy of the subtractor 7 and the determination accuracy of the signal amplifier 2 for expansion of range and the comparator 3, and thus increase in the number of quantization bits will not result in increasing quantization errors of the AD conversion, thus realizing the highly accurate successive comparison AD converter of many bits.

Second Embodiment

FIG. 4 is a schematic circuit diagram to show the second embodiment of the present invention. In FIG. 4, an analog signal to undergo the AD conversion is applied to the input terminal 1 to be input to switch 8. The other input of the switch 8 is connected to second sample hold circuit 6, in which an analog conversion signal after MSB is held. An output of the switch 8 is input to switch 20 and the other input of the switch 20 is connected to the ground potential 27. An output of the switch 20 is connected to first capacitor 23 and the other terminal of the first capacitor 23 is connected to a non-inverting input terminal (+input terminal) of operational amplifier 2. Connected to an inverting input terminal (-input terminal) of the operational amplifier 2 is a common connection point between one terminal of second capacitor 24 and one terminal of third capacitor 25, and the other terminal of the third capacitor 25 is connected to the output of the operational amplifier 2, thus forming a feedback loop of capacitive coupling. The other terminal of the second capacitor 24 is connected to the output of switch 9, one input terminal of the switch 9 is connected to the reference power supply 12, and the other input terminal thereof is connected to the ground potential 27. A control terminal of the switch 9 is controlled by the output of comparator 3, and the signal subtraction operation is carried out here. The output of the operational amplifier 2 is connected through switch 22 to the inverting input terminal of the operational amplifier 2. When a reset control signal 26 becomes active, the operational amplifier 2 is set into a mode of voltage follower of gain 1. A common connection point between the non-inverting input terminal of the operational amplifier 2 and the first capacitor 23 is connected through switch 21 to the ground potential 27. The switch 21 is turned on by a reset control signal 28 to reset the non-inverting input terminal of the operational amplifier 2 to the ground potential 27. The output of the operational amplifier 2 is connected to the non-inverting input terminal of comparator 3 and to switch 11. The reference voltage Vref 12 of the reference power supply is applied to the inverting input terminal of the comparator 3. When the output of the operational amplifier 2 is larger than the reference potential Vref 12, the comparator outputs "H"; when smaller, it outputs "L". This output of the comparator 3 is a quantized output of the input analog signal undergoing successive comparison, and is also the control signal of the switch 9 to control postprocessing (subtraction or doing nothing) of the input analog signal after the AD conversion. The signal having undergone the postprocessing of the input analog signal after the AD conversion passes the switch 11 to be input to the first sample hold circuit 5 and be held as an analog signal for AD conversion of the next bit. The held signal is input through the switch 13 into the second sample hold circuit 6, and the analog signal Vin for AD conversion of the bit after the MSB is circularly fed back from the output of the second sample hold circuit 6 through the switch 8 to the input portion.

The operation in each mode will be described referring to the drawings. The circuit operation in the conversion of MSB will be described referring to FIG. 5 to FIG. 8. In FIG. 4, the switch 8 is flipped to the side of the input terminal 1 to first apply an analog signal to undergo the AD conversion to the input terminal of the switch 20. An equivalent circuit at this time is shown in FIG. 5.

The circuit always has a reset mode prior to the arithmetic operation, to set an initial value of each capacitor. The switch 20 is connected to the ground potential 27, the switch 21 is switched on to be connected to the ground potential 27, and the switch 22 is switched on to short the output and the inverting input terminal of the operational amplifier 2 to fix the operational amplifier 2 in the mode of voltage follower. The switch 9 is connected to the ground potential 27. FIG. 6 is an equivalent circuit diagram upon the reset before the MSB conversion. The both terminals of the first capacitor 23 are connected to the ground potential 27, the inverting input terminal of the operational amplifier 2 is shorted to the output thereof to compose the voltage follower, and the non-inverting input terminal of the operational amplifier 2 is connected to the ground potential 27; therefore, the output of the operational amplifier 2 is also at the same potential as the ground potential 27.

Then the switch 20 is flipped to the side of the input terminal 1 to take in the input analog signal and perform the quantizing operation thereof. This signal input-comparison mode is shown in FIG. 7. The input terminal 1 is connected to one terminal of the first capacitor 23 and the potential of the terminal of the

capacitor changes from the ground potential to that of the analog signal input. Since the switch 21 connected to the other terminal of the capacitor 23 is switched off, the non-inverting input terminal of the operational amplifier 2 is at high impedance and this point becomes floating. Since the potential at this point changes by the same as the change of the potential at the input terminal of the first capacitor 23, the output of the operational amplifier 2 becomes equal to Vin. The comparator 3 receives this Vin to compare it with the reference voltage Vref 12 of the reference power supply, which is the voltage equal to a half of the input analog full range. When Vin is larger than the reference voltage Vref 12, the comparator outputs "H" to determine the quantization code of MSB to be "1". When Vin is smaller than the reference voltage Vref 12, the comparator outputs "L" to determine the quantization code of MSB to be "0". Then the comparator outputs the result to the output terminal 4.

The circuit completes the MSB conversion operation here and moves to the preparation and range expansion operation for conversion of MSB-1. FIG. 8 is an equivalent circuit diagram of the postprocessing and range expansion operation mode. The output 4 of the comparator 3 is connected to the control terminal of the switch 9. When Vin is smaller than the reference voltage Vref 12, "L" is input to the control terminal of the switch 9 and the switch 9 is kept in the connected state to the ground potential 27. At this time, the switch 22 is switched off, so that the third capacitor 25 is connected between the inverting input terminal and the output of the operational amplifier 2. The capacitances of the second capacitor 24 and the third capacitor 25 are set equal to each other. At the same time as the off of the switch 22, the gain of the operational amplifier 2 is set to 2, and thus the operational amplifier 2 doubles the input analog signal Vin used for the conversion of MSB and outputs the doubled signal. At this time, the switch 11 is switched on during the transition of from 1 to 2 of the gain of the operational amplifier 2, and is switched off when the output becomes stable after the setting of the gain to 2. This sampling operation causes the first sample hold circuit 5 to hold the voltage of double Vin used for the comparison of MSB, and the voltage is circularly fed back to the analog input terminal of the AD conversion section upon the quantization operation of the next lower bit. When Vin is larger than the reference voltage Vref 12 of the reference power supply, "H" is input to the control terminal of the switch 9, so that the switch 9 switches the input from the ground potential 27 to the reference voltage Vref 12. At this point, the switch 22 is switched off and thus the third capacitor 25 is connected between the inverting input terminal and the output of the operational amplifier 2. The capacitances of the second capacitor 24 and the third capacitor 25 are set equal to each other. At the same time as the off of the switch 22, the switch 9 also transitions from the ground potential 27 to the reference voltage Vref 12, so that the operational amplifier 2 doubles (Vin-Vref), which is the result of subtraction of Vref from Vin, and outputs the result. At this time, the switch 11 is kept on during a period in which the floating point of the operational amplifier 2 achieves the calculation of Vin-Vref and the gain transitions from 1 to 2, and the switch 11 is switched off when the output becomes stable after the setting of the gain to 2. This sampling operation causes the first sample hold circuit 5 to hold the value of double the voltage resulting from the subtraction of Vref from Vin compared on the occasion of the MSB, and the held voltage is circularly fed back to the analog input terminal of the AD conversion section upon the quantization operation of the next lower bit.

As described above referring to FIG. 5 to FIG. 8, after the MSB conversion using the capacitance-coupled operational amplifier, the input analog signal having undergone the signal amplification with the process gain 1 is compared with the reference voltage Vref 12 and quantized by the comparator 3 and, for the process of the next (MSB-1) bit, the input analog signal undergoes the postprocessing (doing nothing when the quantization code is "0" or performing the subtraction of Vin-Vref when the quantization code is "1") and the range expanding process (doubling the analog signal after the postprocessing to match the signal with the scale for the next (MSB-1) bit which next undergoes the AD conversion) to be circularly fed back through the sample hold circuits to the input.

The architecture after the MSB, particularly the architecture for the AD conversion of (MSB-1) bit will be described using FIG. 9 to FIG. 12.

FIG. 9 illustrates an equivalent circuit during the AD conversion of MSB-1. The switch 8 is flipped to the output side of the second sample hold circuit 6 holding the analog signal voltage for the (MSB-1) bit after the postprocessing and range expansion process, thereby inputting this signal as an analog signal for the next AD conversion. The switch 13 is kept off to maintain the second sample hold circuit 6 in the state holding the analog signal voltage for the (MSB-1) bit.

The circuit always has the reset mode prior to the arithmetic operation, to set the initial value of each capacitor. The switch 20 is connected to the ground potential 27, the switch 21 is on to be connected to the ground potential 27, and the switch 22 is switched on to short the output and inverting input terminal of the operational amplifier 2 to fix the operational amplifier 2 in the mode of voltage follower. The switch 9 is connected to the ground potential 27. FIG. 10 is an equivalent circuit diagram upon the reset before the conversion of MSB-1. The both terminals of the first capacitor 23 are connected to the ground potential 27, the inverting input terminal of the operational amplifier 2 is shorted to the output to keep the operational amplifier 2 as a voltage follower, and the non-inverting input terminal of the operational amplifier 2 is connected to the ground potential 27; therefore, the output of the operational amplifier 2 becomes equal to the ground potential 27.

Then the switch 20 is flipped to the side of the switch 8 (i.e., to the output side of the second sample hold circuit 6) to take in the analog signal voltage for the (MSB-1) bit and quantize it. This analog signal input-comparison mode for the (MSB-1) bit is illustrated in FIG. 11. The output of the second sample hold circuit 6 is connected to one terminal of the first capacitor 23, so that the potential of the terminal changes from the ground potential to the analog signal voltage 29 for the (MSB-1) bit input. Since the switch 21, which is connected to the other terminal of the capacitor 23, is switched off, the non-inverting input terminal of the operational amplifier 2 is at high impedance and this point becomes floating. Since the potential at this point changes by the same as the change of the potential at the input terminal of the first capacitor 23, the output of the operational amplifier 2 becomes equal to the analog signal voltage 29 for the (MSB-1) bit. The comparator 3 receives this analog signal voltage for the (MSB-1) bit and compares it with the reference voltage Vref 12, which is the voltage equal to a half of the input analog full range. When the analog signal voltage for the (MSB-1) bit is larger than the reference voltage Vref 12, the comparator outputs "H" to determine the quantization code of MSB-1 to be "1". When the analog signal voltage for the (MSB-1) bit is smaller than the reference voltage Vref 12, the comparator outputs "L" to determine the quantization code of MSB-1 to be "0". Then the comparator outputs the result to the output terminal 4.

The circuit completes the (MSB-1) bit conversion operation here and, for conversion of the (MSB-2) bit, the circuit moves to the postprocessing and range expansion processing of the (MSB-1) bit analog signal. FIG. 12 is an equivalent circuit diagram of the preparation and range expansion processing mode. The output terminal 4 of the comparator 3 is connected to the control terminal of the switch 9. When the analog signal voltage for the (MSB-1) bit is smaller than the reference voltage Vref 12, "L" is input to the control terminal of the switch 9 to keep the switch 9 in the connected state with the ground potential 27. At this time, the switch 22 is switched off, so that the third capacitor 25 is connected between the inverting input terminal and the output of the operational amplifier 2. The capacitances of the second capacitor 24 and the third capacitor 25 are set equal to each other. At the same time as the off of the switch 22, the gain of the operational amplifier 2 is set to 2, and the operational amplifier 2 thus doubles the analog signal voltage for the (MSB-1) bit used for the conversion of MSB-1 and outputs the result. At this time, the switch 11 is kept on during the transition of from 1 to 2 of the gain of the operational amplifier 2 and is switched off when the output becomes stable after the setting of the gain to 2. This sampling operation causes the first sample hold circuit 5 to hold the voltage equal to double the analog signal voltage for the (MSB-1) bit compared upon the conversion of MSB-1. For circularly feeding the voltage back to the analog input terminal of the AD conversion section upon the quantizing operation of the next lower bit (MSB-2), the analog signal voltage for the (MSB-1) bit held in the first sample hold circuit 5 is transferred to the second hold circuit 6

with the switch 13 being turned on. When the analog signal voltage for the (MSB-1) bit is greater than the reference voltage Vref 12, "H" is input to the control terminal of the switch 9 and thus the switch 9 switches the input from the ground potential 27 to the reference voltage Vref 12. At this point, the switch 22 is switched off, so that the third capacitor 25 is connected between the inverting input terminal and the output of the operational amplifier 2. The capacitances of the second capacitor 24 and the third capacitor 25 are set equal to each other. At the same time as the off of the switch 22, the switch 9 also transitions from the ground potential 27 to the reference voltage Vref 12, and the operational amplifier 2 performs such amplification as to double {(the analog signal voltage for the (MSB-1) bit)-Vref}, which is the result of subtraction of Vref from the analog signal voltage for the (MSB-1) bit. At this time, the switch 11 is kept on during the period in which the floating point of the operational amplifier 2 carries out the calculation of {(the analog signal voltage for the (MSB-1) bit)-Vref} and in which the gain transitions from 1 to 2, and is switched off when the output becomes stable after the setting of the gain to 2. This sampling operation causes the first sample hold circuit 5 to hold the value of double the voltage resulting from the subtraction of Vref from the analog signal voltage for the (MSB-1) bit compared upon the conversion of MSB-1. For circularly feeding the value back to the analog input terminal of the AD conversion section upon the quantizing operation of the next lower bit MSB-2, the switch 13 is switched on to transfer the analog signal voltage for the (MSB-1) bit held in the first sample hold circuit 5, to the sample hold circuit 6.

As described above referring to FIG. 9 to FIG. 12, upon the AD conversion of the (MSB-1) bit using the capacitance-coupled operational amplifier, the input analog signal after the signal amplification with the process gain 1 is compared with the reference voltage Vref 12 and quantized by the comparator 3 and, for processing of the next bit (MSB-2), the analog signal voltage for the (MSB-1) bit undergoes the postprocessing (doing nothing when the quantization code is "0" or performing the subtraction of {(the analog signal voltage for the (MSB-1) bit)-Vref} when the quantization code is "1") and the range expanding process (doubling the analog signal after the postprocessing to match the signal with the scale for the next bit (MSB-2) which next undergoes the AD conversion) and the result is circularly fed back through the sample hold circuits to the input.

The analog signal circuit having undergone the AD conversion in this way is subjected to the range expanding operation, the loop feedback, and again the AD conversion, thus enabling highly accurate successive comparison by the simple circuit configuration. Namely, the present embodiment does not necessitate the DA converter 54 as shown in FIG. 1. With increase in the number of quantization bits of the AD conversion, it was difficult for the circuit shown in FIG. 1 to achieve high accuracy because the accuracy of the AD conversion was determined by the conversion accuracy of the DA converter 54; whereas, in the present embodiment, the accuracy of the AD conversion is determined only by the operation accuracy of the capacitance-coupled operational amplifier and the determination accuracy of the comparator, so that the increase in the number of quantization bits will not result in increasing the quantization errors of the AD conversion, thus realizing the highly accurate successive comparison AD converter of many bits. In the successive comparison AD converter of FIG. 1, the increase in the number of quantization bits resulted in also increasing the number of bits of the internal DA converter 54 to N bits, which increased the circuit scale. In contrast, with the circuit of the present embodiment, the increase in the number of quantization bits does not result in increasing the circuit scale, so that the successive comparison AD converter can be constructed in high integration and with low power consumption.

As detailed above, the present invention realizes the AD converter for successive conversion from the MSB to carry out the following processing by simple hardware: the analog signal after the AD conversion by the signal amplifier and sample hold circuits is subjected to the subtraction and range expanding processes based on the quantization result of a bit of interest to be converted to a processable analog voltage of the next bit and the voltage is fed back to the input to carry out the AD conversion of the next bit, thus permitting the highly accurate successive comparison AD conversion operation by the simple circuit configuration. The circuit is a flexible circuit without increase of the hardware against increase in the

number of quantization bits, thus achieving the successive comparison AD converter in high integration and with low power consumption.

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Claims of corresponding document: **US6259393**

What is claimed is:

1. A semiconductor integrated circuit comprising:
signal amplifying means capable of switching a gain to 1 or 2;
arithmetic processing means connected to an input side of the signal amplifying means, said arithmetic processing means carrying out a subtraction process of a reference voltage from a signal input thereto to output a result of the subtraction process, or outputting the signal input thereto without performing the subtraction process;
changeover means having one changeover terminal connected to a signal input terminal and having another changeover terminal connected to an output side of sample hold means, and having a common terminal of connected to an input side of said arithmetic processing means;
a comparator connected to an output side of said signal amplifying means, said comparator comparing an output from said signal amplifying means with the reference voltage to binarize the output; and
switch means connecting the output side of said signal amplifying means to an input side of said sample hold means;
wherein said arithmetic processing means carries out a changeover, based on an output from said comparator, so that the subtraction of the reference voltage from the signal input is performed to output the result when the output from said signal amplifying means is larger than the reference voltage, and the signal input is outputted without performing the subtraction when the output from said signal amplifying means is not larger than the reference voltage, and
said signal amplifying means amplifies twice the signal resulting from the subtraction of the signal outputted without the subtraction, when the signal inputted into said comparator is not greater than the reference voltage.

2. The semiconductor integrated circuit according to claim 1, wherein the gain of said signal amplifying means is set to 1 in an MSB conversion mode where said changeover means electrically connects said signal input terminal to the input side of said arithmetic processing means.

3. The semiconductor integrated circuit according to claim 1, wherein the gain of said signal amplifying means is set to 2 in a conversion mode except for an MSB conversion mode, where the changeover means electrically connects the output side of said sample hold means to the input side of said arithmetic processing means.

4. The semiconductor integrated circuit according to claim 1, wherein after such an operation that a signal before AD conversion is applied to said signal input terminal, that the signal is amplified by a factor of 1 or 2 by said signal amplifying means, and that a binary comparison operation of said comparator is completed,
said switch means is switched on, whereby either after execution of the subtraction process of subtracting a signal of said reference voltage from said signal before the AD conversion when the output of the comparator is active or after execution of an arithmetic process of not performing the subtraction process of the signal of said reference voltage from said signal before the AD conversion when the output of the comparator is non-active, an output from said signal amplifying means is supplied to said sample hold

means.

5. The semiconductor integrated circuit according to claim 1, wherein when said switch means is first switch means, said sample hold means comprises a first hold circuit and a second hold circuit connected through second switch means thereto, wherein when the first switch means is on, the second switch means is off, and wherein when said first switch means is off, the second switch means is on.

6. A semiconductor integrated circuit comprising:
signal amplifying means capable of switching a gain to 1 or 2 and capable of performing a changeover between performing a subtraction process of a reference voltage from a signal input thereto to output a result of said subtraction process and outputting the signal input thereto without performing the subtraction process;
changeover means who one changeover terminal is connected to a signal input terminal and whose other changeover terminal is connected to an output side of sample hold means, a common terminal of said changeover means being connected to an input side of said signal amplifying means;
a comparator connected to an output side of said signal amplifying means, said comparator comparing an output from said signal amplifying means with the reference voltage to binarize the output; and
switch means connecting the output side of said signal amplifying means to an input side of said sample hold means;
wherein said signal amplifying means carries out the changeover between performing the subtraction process of the reference voltage from the signal input thereto to output the result and outputting the signal input thereto without performing the subtraction process, based on an output from said comparator.

7. The semiconductor integrated circuit according to claim 6, wherein the gain of said signal amplifying means is set to 1 in an MSB conversion mode where said changeover means electrically connects said signal input terminal to the input side of said signal amplifying means.

8. The semiconductor integrated circuit according to claim 6, wherein the gain of said signal amplifying means is set to 2 in a conversion mode except for an MSB conversion mode, where the changeover means electrically connects the output side of said sample hold means to the input side of said signal amplifying means.

9. The semiconductor integrated circuit according to claim 6, wherein after such an operation that a signal before AD conversion is applied to said signal input terminal, that the signal is amplified by a factor of 1 or 2 by said signal amplifying means, and that a binary comparison operation of said comparator is completed,
said switch means is switched on, whereby either after execution of the subtraction process of subtracting a signal of said reference voltage from said signal before the AD conversion when the output of the comparator is active or after execution of an arithmetic process of not performing the subtraction process of the signal of said reference voltage from said signal before the AD conversion when the output of the comparator is not-active, an output from said signal amplifying means is supplied to said sample hold means.

10. The semiconductor integrated circuit according to claim 6, wherein when said switch means is first switch means, said sample hold means comprises a first hold circuit and a second hold circuit connected through second switch means thereto, wherein when the first switch means is on, the second switch means is of, and wherein when said first switch means is off, the second switch means is on.

11. A method for driving a semiconductor integrated circuit comprising:
signal amplifying means capable of switching a gain to 1 or 2;
arithmetic processing means connected to an input side of the signal amplifying means, said arithmetic

processing means carrying out a subtraction process of a reference voltage from a signal input thereto to output a result of the subtraction process, or outputting the signal input thereto without performing the subtraction process;
changeover means having one changeover terminal connected to a signal input terminal and having another changeover terminal connected to an output side of sample hold means, and having a common terminal connected to an input side of said arithmetic processing means;
a comparator connected to an output side of said signal amplifying means, said comparator comparing an output from said signal amplifying means with the reference voltage to binarize the output; and
switch means connecting the output side of said signal amplifying means to an input side of said sample hold means;
wherein said arithmetic processing means carries out a changeover, based on an output from said comparator, so that the subtraction of the reference voltage from the signal input is performed to output the result when the output from said signal amplifying means is larger than the reference voltage, and the signal input is outputted without performing the subtraction when the output from said signal amplifying means is not larger than the reference voltage, and
wherein said signal amplifying means amplifies twice the signal resulting from the subtraction of the signal input into said arithmetic processing means, or the signal outputted without the subtraction when the signal inputted into said comparator is not greater than the reference voltage, and
said driving method comprising an MSB (Most Significant Bit) conversion mode in which the gain of said signal amplifying means is set to 1, and said changeover means electrically connects said signal input terminal to the input side of said arithmetic processing means or said signal amplifying means.

12. The method according to claim 11, wherein in a conversion mode except for said MSB conversion mode, the gain of said signal amplifying means is set to 2.

13. The driving method according to claim 11, comprising a step wherein after such an operation that a signal before AD conversion is applied to said signal input terminal, that the signal is amplified by a factor of 1 or 2 by said signal amplifying means, and that a binary comparison operation of said comparator is completed,
said switch means is switched on, whereby either after execution of the subtraction process of subtracting a signal of said reference voltage from said signal before the AD conversion when the output of the comparator is active or after execution of an arithmetic process of not performing the subtraction process of the signal of said reference voltage from said signal before the AD conversion when the output of the comparator is non-active, an output from said signal amplifying means is supplied to said sample hold means.

14. The driving method according to claim 11, wherein when said switch means is first switch means, said sample hold means comprises a first hold circuit and a second hold circuit connected through second switch means thereto, wherein when the first switch means is on, the second switch means is off, and wherein when said first switch means is off, the second switch means is on.

15. A method for driving a semiconductor integrated circuit comprising:
signal amplifying means capable of switching a gain and capable of performing a changeover between performing a subtraction process of a reference voltage from a signal input thereto to output a result of said subtraction process and outputting the signal input thereto without performing the subtraction process;
changeover means whose one changeover terminal is connected to a signal input terminal and whose other changeover terminal is connected to an output side of sample hold means, a common terminal of said changeover means being connected to an input side of said signal amplifying means;
a comparator connected to an output side of said signal amplifying means, said comparator comparing an output from said signal amplifying means with the reference voltage to binarize the output; and
switch means connecting the output side of said signal amplifying means to an input side of said sample

hold means;
wherein said signal amplifying means carries out the changeover between performing the subtraction process of the reference voltage from the signal input thereto to output the result and outputting the signal input thereto without performing the subtraction process, based on an output from said comparator,
said driving method comprising an MSB (Most Significant Bit) conversion mode in which the gain of said signal amplifying means is set to 1 and said changeover means electrically connected said signal input terminal to the input side of said signal amplifying means.

16. The method according to claim 15, wherein in a conversion mode except for said MSB conversion mode, the gain of said signal amplifying means is set to 2.

17. The driving method according to claim 15, comprising a step wherein after such an operation that a signal before AD conversion is applied to said signal input terminal, that the signal is amplified by a factor of 1 or 2 by said signal amplifying means, and that a binary comparison operation of said comparator is completed,
said switch means is switched on, whereby either after execution of the subtraction process of subtracting a signal of said reference voltage from said signal before the AD conversion when the output of the comparator is active or after execution of an arithmetic process of not performing the subtraction process of the signal of said reference voltage from said signal before the AD conversion when the output of the comparator is non-active, an output from said signal amplifying means is supplied to said sample hold means.

18. The driving method according to claim 15, wherein when said switch means is first switch means, said sample hold means comprises a first hold circuit and a second hold circuit connected through second switch means thereto, wherein when the first switch means is on, the second switch means is off, and wherein when said first switch means is off, the second switch means is on.

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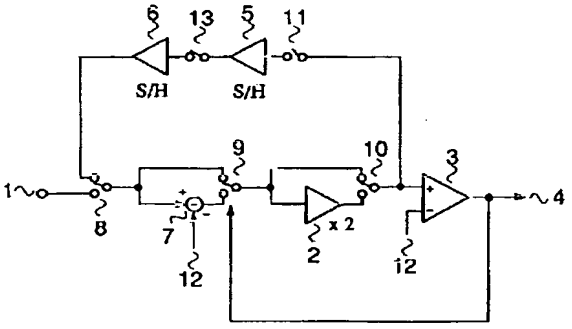
最終頁に続く

(54)【発明の名称】　半導体集積回路

(57)【要約】
【課題】　ＤＡコンバーターを用いていたので回路規模が増加、消費電力の増大を招いていた。
【解決手段】　利得を１倍又は２倍に切換え可能な信号増幅手段２，１０と、入力される信号と基準電圧とを減算処理して出力するか又は減算処理しないで出力する演算処理手段７，９と、一方の切換端子が信号入力端子と接続され且つ他方の切換端子がサンプルホールド手段５，６の出力側と接続され、共通端子が演算処理手段の入力側に接続される切換手段８と、信号増幅手段の出力と基準電圧と比較して２値化するコンパレーター３と、信号増幅手段の出力側とサンプルホールド手段の入力側とを接続するスイッチ手段１１と、を有し、演算処理手段はコンパレーターの出力に基づいて、入力される信号と基準電圧とを減算処理して出力するか、減算処理しないで出力するか、の切換えを行う。



【特許請求の範囲】

【請求項１】　利得を１倍又は２倍に切換え可能な信号増幅手段と、

該信号増幅手段の入力側に接続される、入力される信号と基準電圧とを減算処理して出力するか又は入力される信号を減算処理しないで出力する演算処理手段と、

一方の切換端子が信号入力端子と接続され且つ他方の切換端子がサンプルホールド手段の出力側と接続され、共通端子が前記演算処理手段の入力側に接続される切換手段と、

前記信号増幅手段の出力側に接続され、前記信号増幅手段の出力と基準電圧と比較して２値化するコンパレーターと、

前記信号増幅手段の出力側と前記サンプルホールド手段の入力側とを接続するスイッチ手段と、を有し、

前記演算処理手段は、前記コンパレーターの出力に基づいて、入力される信号と基準電圧とを減算処理して出力するか、入力される信号を減算処理しないで出力するか、の切換えを行ってなる半導体集積回路。

【請求項２】　利得を１倍又は２倍に切換え可能であって、入力される信号と基準電圧とを減算処理して出力するか又は減算処理しないで出力するかの切換えが可能な信号増幅手段と、

一方の切換端子が信号入力端子と接続され且つ他方の切換端子がサンプルホールド手段の出力側と接続され、共通端子が前記信号増幅手段の入力側に接続される切換手段と、

前記信号増幅手段の出力側に接続され、前記信号増幅手段の出力と基準電圧と比較して２値化するコンパレーターと、

前記信号増幅手段の出力側と前記サンプルホールド手段の入力側とを接続するスイッチ手段と、を有し、

前記信号増幅手段は、前記コンパレーターの出力に基づいて、入力される信号と基準電圧とを減算処理して出力するか、入力される信号を減算処理しないで出力するか、の切換えを行ってなる半導体集積回路。

【請求項３】　前記切換手段が、前記信号入力端子と前記演算処理手段又は前記信号増幅手段の入力側とを導通させるＭＳＢ変換モードにおいて、前記信号増幅手段の利得が１に設定されることを特徴とする請求項１又は請求項２に記載の半導体集積回路。

【請求項４】　前記切換手段が、前記サンプルホールド手段の出力側と前記演算処理手段又は前記信号増幅手段の入力側とを導通させる、ＭＳＢ変換モード以外の変換モードにおいて、前記信号増幅手段の利得が２に設定されることを特徴とする請求項１又は請求項２に記載の半導体集積回路。

【請求項５】　前記信号入力端子にＡＤ変換前の信号が印加され、前記信号増幅手段によって１又は２倍され、前記コンパレーターの２値比較動作が終了した後に、該コンパレーターの出力がアクティブの時に、前記ＡＤ変換前の信号から前記基準電圧分の信号を減算処理し、該コンパレーターの出力がノンアクティブの時に、前記ＡＤ変換前の信号から前記基準電源分の信号を減算処理しない演算処理実行後、前記信号増幅手段の出力を前記スイッチ手段を導通させて前記サンプルホールド手段に入力させることを特徴とする請求項１又は請求項２に記載の半導体集積回路。

【請求項６】　前記スイッチ手段を第一のスイッチ手段としたときに、

前記サンプルホールド手段を、第一のホールド回路と第二のスイッチ手段を介してつながった第二のホールド回路から構成し、該第一のスイッチ手段がオンの時、該第二のスイッチ手段がオフし、該第一のスイッチ手段がオフの時、該第二のスイッチ手段がオンすることを特徴とする請求項１又は請求項２に記載の半導体集積回路。

【請求項７】　前記切換手段を第一の切換手段とし、前記基準電圧を第一の基準電圧としたときに、

前記信号増幅手段が演算増幅器より構成され、該演算増幅器の非反転入力端子は第一の容量手段を介して第二の切換手段の共通端子と接続され、該第二の切換手段の一方の切換端子は第二の基準電圧が印加され、他方の切換端子は該第一の切換手段の共通端子と接続されており、反転入力端子は第二の容量手段を介して第三の切換手段の共通端子と接続され且つ第三の容量手段を介して該演算増幅器の出力と接続されており、該第三の切換手段の一方の切換端子は第二の基準電圧が印加され、他方の切換端子は第一の基準電圧が印加されており、該第三の切換手段は、前記コンパレーターの２値出力でコントロールされることを特徴とする請求項２に記載の半導体集積回路。

【請求項８】　前記第三の切換手段は、前記コンパレーターの出力がアクティブの時は前記第一の基準電圧が印加された切換端子と接続され、ノンアクティブの時は前記第二の基準電圧が印加された切換端子と接続されることを特徴とする請求項７に記載の半導体集積回路。

【請求項９】　前記演算増幅器の前記非反転入力端子は第三のスイッチ手段を介して前記第二の基準電圧が印加され、前記演算増幅器の前記反転入力端子が第四のスイッチ手段を介して前記演算増幅器の出力側と接続されていることを特徴とする請求項７に記載の半導体集積回路。

【請求項１０】　前記スイッチ手段を第一のスイッチ手段としたときに、該第一のスイッチ手段がオフし、前記第二の切換手段及び第三の切換手段が前記第二の基準電圧に接続され、第三のスイッチ手段がオンし前記非反転入力端子に前記第二の基準電圧が印加され、該第四のスイッチ手段がオンし、前記反転入力端子と前記演算増幅器の出力側が接続されるリセットモードを設けることを特徴とする請求項９に記載の半導体集積回路。

【請求項１１】　前記第二の切換手段の切換端子が前記第一の切換手段の共通端子に接続され、前記第三及び第四のスイッチ手段がオフし、前記第一の切換手段より信号が入力される量子化前処理モードを設けることを特徴とする請求項７に記載の半導体集積回路。

【請求項１２】　前記量子化前処理モード後、前記演算増幅器の出力結果を前記コンパレーターが２値化処理し、量子化コードを出力する量子化モードを設けることを特徴とする請求項１１に記載の半導体集積回路。

【請求項１３】　前記コンパレーターの結果より前記第三の切換手段を制御し、前記演算増幅器で得た演算結果を第二のスイッチ手段はオフし第一のスイッチ手段をオンし、第一のホールド回路のみに該演算結果を書き込む量子化後処理モードを設けることを特徴とする請求項１２に記載の半導体集積回路。

【請求項１４】　第一のスイッチ手段をオフし、第二のスイッチ手段をオンすることにより第一のホールド回路に書き込まれた該演算結果を、第二のホールド回路に転送することを特徴とする請求項７又は請求項１３に記載の半導体集積回路。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は半導体集積回路に係わり、特に逐次比較型ＡＤ変換器に関するものである。

【０００２】

【従来の技術】現在のデジタル信号処理の発達でアナログ信号を、デジタル信号に変換するＡＤ変換器は重要な技術であり、多様な方式のＡＤ変換器（以下、ＡＤコンバーターと略す。）が開発されてきた。特に高速度用途では、量子化範囲のすべてに対応する比較電圧がありＮビット変換の場合、２Ｎ－１個のコンパレーターを持ち同時並列に比較エンコードするフラッシュＡＤコンバーターが主流であるがコンパレーターの数が多い為、低消費電力が要求される携帯用端末等の用途には不向きであった。そこで低消費電力である逐次比較型ＡＤコンバーターが多く利用されている。

【０００３】図１２に従来の逐次比較型ＡＤコンバーターのブロック図を示す。変換されるアナログ信号は入力端子５０に印加され、コンパレーター５１の＋入力端子に入る。コンパレーター５１の－入力端子は逐次比較レジスタ５３で入力ビットが設定され、比較アナログ電圧を発生するＤＡコンバーター５４の出力が接続される。制御回路５２はコンパレーター５１の結果を元に逐次比較制御レジスタ５３の値を設定しＤＡコンバーター５４の出力をコントロールする。逐次比較型ＡＤコンバーターの場合、ＭＳＢより１ビットずつ、順番にデジタルコードに変換してゆく。Ｎビットの逐次比較を考えると、制御回路５２からのコントロール信号により逐次比較レジスタＭＳＢであるＮビット目を１に、他のビットを０に設定する。このコードがＤＡコンバーター５４に加えられアナログ比較信号Ｖｄａに変換される。この場合、全量子化範囲の１／２の電圧が発生し、入力端子５０に印加されたアナログ入力信号Ｖｉｎと比較する。Ｖｉｎ＞Ｖｄａの場合、コンパレーター５１の出力は“Ｈ”となり、制御回路５２に送られる。制御回路５２では、“Ｈ”を受け取ると、逐次比較レジスタの内容を、現在の比較したビットであるＭＳＢを１に保ったまま下位ビットＭＳＢ－１を１に設定し、ＤＡコンバーター５４に送る。この場合、ＭＳＢビットの１は確定し、ＭＢＳ－１ビットに１を立てて、次の比較動作を行う。Ｖｉｎ＜Ｖｄａの場合、コンパレーター５１の出力は“Ｌ”となり、制御回路５２に送られる。制御回路５２では、“Ｌ”を受け取ると、逐次比較レジスタの内容を、現在の比較したビットであるＭＳＢを１から０に変更しかつ、下位ビットＭＳＢ－１を１に設定し、ＤＡコンバーター５４に送る。この場合、ＭＳＢビットの０は確定し、ＭＳＢ－１ビットに１を立てて、次の比較動作を行う。この動作を上位ビットから順に下位ビットに向けて、比較・レジスタ設定を繰り返すことで、最終的に逐次比較レジスタの内容が入力端子５０に印加されたアナログ入力信号ＶｉｎをＡＤ変換した２進コードとなる。

【０００４】

【発明が解決しようとする課題】しかしながら、従来のビット数の多い逐次比較型ＡＤコンバーターを構成しようとした場合、図１２で示した逐次比較型ＡＤコンバーターではアナログ比較電圧を発生するＤＡコンバーター５４のビット数も同数必要となり、回路規模が増加し、これによる消費電力の増大を招いていた。また、逐次変換方式ＡＤコンバーターの変換精度はＤＡコンバーター５４の誤差が主要因であり、ビット数の増加はＤＡコンバーター５４の精度を悪化させ、結果的にＡＤコンバーターとして、単調性を欠いたりコード抜けが発生する要因となっていた。

【０００５】

【課題を解決するための手段及び作用】以下、本発明の構成について図１及び図３を参照しつつ説明する。ただし、本発明は図１及び図３の構成のみに限定されるものではない。

【０００６】本発明は、利得を１倍又は２倍に切換え可能な信号増幅手段（図１の２，１０）と、該信号増幅手段の入力側に接続される、入力される信号と基準電圧とを減算処理して出力するか又は入力される信号を減算処理しないで出力する演算処理手段（図１の７，９）と、一方の切換端子が信号入力端子（図１の１）と接続され且つ他方の切換端子がサンプルホールド手段（図１の５，６）の出力側と接続され、共通端子が前記演算処理手段の入力側に接続される切換手段（図１の８）と、前記信号増幅手段の出力側に接続され、前記信号増幅手段の出力と基準電圧（図１の１２）と比較して２値化するコンパレーター（図１の３）と、前記信号増幅手段の出

力側と前記サンプルホールド手段の入力側とを接続するスイッチ手段（図１の１１）と、を有し、前記演算処理手段（図１の７，９）は、前記コンパレーター（図１の３）の出力に基づいて、入力される信号と基準電圧とを減算処理して出力するか、入力される信号を減算処理しないで出力するか、の切換え（図１の９の切換え）を行ってなる半導体集積回路を提供するものである。

【０００７】また本発明は、利得を１倍又は２倍に切換え可能であって、入力される信号と基準電圧とを減算処理して出力するか又は減算処理しないで出力するかの切換えが可能な信号増幅手段（図３の２）と、一方の切換端子が信号入力端子（図３の１）と接続され且つ他方の切換端子がサンプルホールド手段（図３の５，６）の出力側と接続され、共通端子が前記信号増幅手段の入力側に接続される切換手段（図３の８）と、前記信号増幅手段の出力側に接続され、前記信号増幅手段の出力と基準電圧（図３の１２）と比較して２値化するコンパレーター（図３の３）と、前記信号増幅手段の出力側と前記サンプルホールド手段の入力側とを接続するスイッチ手段（図３の１１）と、を有し、前記信号増幅手段（図３の２）は、前記コンパレーター（図３の３）の出力に基づいて、入力される信号と基準電圧とを減算処理して出力するか、入力される信号を減算処理しないで出力するか、の切換え（図３の９の切換え）を行ってなる半導体集積回路を提供するものである。

【０００８】すなわち、本発明によれば入力アナログ信号を基準電源の基準電圧（１２）と比較し、その結果を元に該入力アナログ信号を、そのまま又は基準電圧値を引いた差分値を入力にフィードバックすることで、逐次変換動作を実現できる為、コンパレーターのみを使用し、ＤＡコンバーターのいらないシンプルな回路が低消費電力で実現できる。これにより変換ビット数が増加してもハードウェアの増加の無い高精度な逐次変換ＡＤコンバーターを可能とした。

【０００９】また本発明において、該第一の切換手段（８）が該信号入力端子（１）と演算処理手段（図１の７，９）又は前記信号増幅手段（図３の２）の入力側とを導通させるＭＳＢ変換モードにおいて、該信号増幅手段（２）の利得が１に設定され、該第一の切換手段が該信号入力端子と該サンプルホールド回路の該出力を導通させる、ＭＳＢ以外の変換モードにおいて、該信号増幅手段の利得が２に設定されることを特徴とする、半導体集積回路を提供する。

【００１０】すなわち本発明によれば、ＭＳＢ変換モードとＭＳＢ以外の変換モードにおいて、該信号増幅手段の利得を切り替えるだけで、各ビット変換モードに対応でき回路素子数を低減した逐次比較ＡＤコンバーターを実現した。

【００１１】また本発明において、該信号入力端子（１）にＡＤ変換前の信号が印加され、該信号増幅手段（２）によって１又は２倍され、該コンパレーター（３）の２値比較動作が終了した後に、該コンパレーターの出力がアクティブの時、該ＡＤ変換前の信号から該基準電源分の信号を減算処理し、該コンパレーターの出力がノンアクティブの時、該ＡＤ変換前の信号から該基準電源分の信号を減算処理しない演算処理実行後、該信号増幅手段の出力を第一のスイッチ手段（１１）を導通させ該サンプルホールド回路（５）に入力されることを特徴とする半導体集積回路を提供する。

【００１２】すなわち本発明によれば１個のコンパレーターすなわち１ビットのＡＤコンバーターにより、量子化した結果をもとに変換される入力アナログ信号に適応した処理を行い、次の変換ビットの入力情報として保持して置くことで、変換ビット数が増えてもハード的には、１ビットのＡＤコンバーターのみで実現することができ、変換ビット数が増加しても高精度なＡＤ変換が可能となった。

【００１３】また、本発明によれば、該信号増幅手段が演算増幅器（図３の２）より構成され、該演算増幅器の非反転入力端子が第一の容量手段（図３の２３）を介して第二の切換手段（図３の２０）と接続され、該第二の切換手段の一方は第二の基準電源（図３の２７）に接続され、他方は該第一の切換手段（図３の８）の出力と接続されており、反転入力端子は第二の容量手段（図３の２４）を介して第三の切換手段（図３の９）と接続されかつ、第三の容量手段（図３の２５）を介して該演算増幅器の出力とも接続されており、該第三の切換手段の一方は、接地電位（図３の２７）と、他方は第一の基準電源（図３の１２）と接続された構成となっており、該第三の切換手段は、該コンパレーターの２値出力でコントロールされることを特徴とする半導体集積回路を提供する。

【００１４】すなわち本発明によれば、演算増幅器の非反転入力端子に接続されている第一の容量手段を介して、基準電圧値と入力信号値を交互に書き込むことで該基準電圧値からの入力電圧値の差分を正確に入力することを可能とし、該演算増幅器等のオフセットの影響を受けない正確な信号処理を可能とした。また該演算増幅器の反転端子に接続された第二の容量手段を介して接地電位又は基準電圧値に接続されるスイッチ（切換手段）を持ち、リセット時には基準電圧値に、ＡＤ変換後は該コンパレーターすなわち１ビットＡＤコンバーターの出力結果により、該基準電圧値か接地電位のいずれかに接続することにより、比較された入力アナログ信号の下位ビットへの変換動作がシンプルな制御と回路構成で実現できる為、レンジ変換の精度を大幅に向上することが可能となり、逐次比較型ＡＤコンバーターの量子化変換ビット数を大幅に増大することを可能とした。

【００１５】また本発明によれば、該第三の切換手段（図３の９）が該コンパレーター（図３の３）の２値出

力がアクティブの時、該第一の基準電源（図3の12）と接続され、ノンアクティブの時、接地電位（図3の27）と接続されることを特徴とする半導体集積回路を提供する。

【0016】すなわち本発明によれば、ビット変換結果に応じて、ビット出力が“H”ならば入力アナログ信号からフルレンジの半分の電圧を引き帰還ループに戻し、ビット出力が“L”ならば入力アナログ信号は無処理のまま該帰還ループに戻すことにより、次のビット出力の比較の為に必要な減算処理等を、容量結合された演算増幅器1段のみで可能とし、精度の向上はもちろんのこと、特別な回路を必要とせず処理回路を実現したことにより、低消費電力化も可能となった。

【0017】この様に本発明によれば、容量結合型演算増幅器とサンプルホールド回路及び1ビットの量子化コンパレーターを用いて、上位ビットのＭＳＢから順に量子化判定後、その量子化結果に基ずき入力アナログ信号に減算処理、レンジ拡大処理を行い、処理後のアナログ信号を入力に帰還し、次のビットの量子化動作を行う信号巡回回路構成を取ることにより、1段の容量結合型演算増幅器とサンプルホールド回路という簡単な構成でアナログ処理を高精度化したことで回路規模が小さい高集積化が可能でかつ低消費電力が実現でき、量子化変換誤差を飛躍的に改善した多ビット長の逐次比較型ＡＤ変換器を実現できる。

【0018】

【実施例】以下、本発明による実施例について、図面を参照しつつ詳細に説明する。

［第1の実施例］図1は、本発明の第1の実施例を示す回路図である。図1において入力端子1に、ＡＤ変換されるアナログ信号が印加され、スイッチ手段8，9，10を通ってコンパレーター3の非反転入力端子（＋入力端子）に入力される。コンパレーター3の反転入力端子（－入力端子）には、基準電源12から基準電圧が印加されており、入力端子1に印加されたアナログ信号が基準電源12の基準電圧よりも大きいときはコンパレーター3の出力は“H”に、小さいときはコンパレーター3の出力は“L”になる。なお基準電源12は、ＡＤ変換するアナログ信号の取りうる電圧フルレンジVfullの1／2の電圧値（Vref）を持った直流電圧源である。すなわち、Vref＝Vfull／2の関係にある。本実施例における逐次比較型ＡＤコンバーターは最上位桁ＭＳＢより逐次ＡＤ変換されていくので、上記説明の動作は、ＭＳＢ時変換の時のモードである。入力端子1に印加されたアナログ信号が基準電源12の基準電圧よりも大きくコンパレーター3の出力が“H”のとき、ＭＳＢの量子化値を1に決定すると共に、スイッチ手段9を制御し入力端子1に印加されたアナログ信号から基準電源12の基準電圧値を引く減算処理回路7の出力をスイッチ9の出力とする。

【0019】次に下位ビットのＡＤ変換の為の前処理として、減算処理をしたアナログ信号を2倍増幅する信号増幅手段2を通って、信号を2倍増幅しレンジ拡大処理を行いスイッチ手段10の出力とする。入力端子1に印加されたアナログ信号が基準電源12の基準電圧よりも小さくコンパレーター3の出力が“L”の時、ＭＳＢの量子化値を0に決定すると共に、スイッチ手段9を制御し入力端子1に印加されたアナログ信号を、そのままスイッチ手段9の出力とする。次に下位ビットのＡＤ変換の為の前処理として、スイッチ手段9の出力であるアナログ信号を2倍増幅する信号増幅手段2を通って、信号を2倍増幅しレンジ拡大処理を行いスイッチ手段10の出力とする。この様に下位ビット変換用に加工されたアナログ信号はスイッチ手段11を介して第一のサンプルホールド回路（Ｓ／Ｈ）5に入力され一時保持される。ＡＤ変換処理部での量子化動作が終了するとスイッチ手段11をオフ、スイッチ手段13をオンし、サンプルホールド回路5に保持されていた、次のビットのＡＤ変換用のアナログ信号を第二のサンプルホールド回路（Ｓ／Ｈ）6に入力し、スイッチ手段13をオフすることでこの値を保持する。スイッチ手段8はサンプルホールド回路6の出力をＡＤ変換処理部へ入力するモードとなり、ＭＳＢ以外のビットの処理は、サンプルホールド回路6の出力がスイッチ手段8の出力になる様に設定される。すなわちＭＳＢ以外の処理ではＡＤ変換処理部の出力信号は、サンプルホールド回路5，6を介してＡＤ変換処理部の入力に帰還される。

【0020】図2は本実施例のＡＤ変換アーキテクチャーの説明図である。図2の説明は例として3ビットの本実施例における逐次比較型ＡＤコンバーターの場合であるが、本発明によるＡＤコンバーターはむろん、このビット数に限ったものでは無い。

【0021】図1の入力端子1に印加されるアナログ信号を図2の14に示す。119はＭＳＢにおける入力アナログ信号の量子化レンジであり、量子化範囲は3ビットすなわち8通りに等分割それぞれの量子化範囲に量子化代表点000から111までが割り当てられている。図1のコンパレーターの基準電源12の基準電位、すなわちVrefは量子化レンジ119の中心に位置し、この値を超えた場合、図1のコンパレーター3の出力は“H”になりＭＳＢの量子化コードは“1”に確定する。入力アナログ信号がこの値を超えなかった場合、コンパレーター3の出力は“L”となりＭＳＢの量子化コードは“0”に確定する。図2の例では、入力アナログ信号14が基準電位Vref12よりも小さい為、コンパレーター（Comp）3の出力は“L”となり、ＭＳＢの“0”が確定する。

【0022】次に下位ビットであるＭＳＢ－1ビットの量子化を行う為、ＭＳＢにおけるアナログ信号が基準電位Vref12を超えずコンパレーター3の出力は“L”

であったので、図１の減算処理回路７は通さず、２倍のゲインを持った信号増幅手段２によりアナログ増幅され、２倍のレンジ拡大を行い図２の１５に示すアナログ信号となり、図１のサンプルホールド回路５，６を介してＡＤ変換処理部の入力に帰還され、ＭＳＢ－１の位としてＡＤ変換される。この時、レンジ拡大後の信号である為、ＡＤ変換処理部に入力された図２のアナログ信号１５に対応する量子化レンジ１２０はＭＳＢ時の量子化レンジ１１９の基準電位Ｖref１２以下のレベルを２倍したものとなり、ＭＳＢ－１の位の量子化を実現している。量子化レンジ１２０は量子化レンジ１１９に対して２倍にレンジに拡大されているので、フルレンジを４通りに分割した量子化範囲をもち、図１のコンパレーター３の基準電源の基準電位Ｖref１２は量子化レンジ１２０の中心に位置し、この値を超えた場合、図１のコンパレーター３の出力は“Ｈ”になりＭＳＢ－１の量子化コードは“１”に確定する。入力アナログ信号がこの値を超えなかった場合、コンパレーター３の出力は“Ｌ”となりＭＳＢ－１の量子化コードは“０”に確定する。図２の例では、入力アナログ信号１５が基準電位Ｖref１２よりも大きい為、コンパレーター３の出力は“Ｈ”となり、ＭＳＢ－１の“１”が確定する。

【００２３】次に下位ビットであるＭＳＢ－２ビットの量子化を行う為、ＭＳＢ－１におけるアナログ信号１５が基準電位Ｖref１２を超えコンパレーター３の出力は“Ｈ”であったので、図１の減算処理回路７に入力されアナログ信号１５から基準電源Ｖref１２に相当するアナログ信号１６の部分を減じたアナログ信号１７は、２倍のゲインを持った信号増幅手段２によりアナログ増幅され、２倍のレンジ拡大を行い図２に示すアナログ信号１８となり、図１のサンプルホールド回路５，６を介してＡＤ変換処理部の入力に帰還され、ＭＳＢ－２（ＬＳＢ）の位としてＡＤ変換される。この時、レンジ拡大後の信号である為、ＡＤ変換処理部に入力された図２のアナログ信号１８に対応する量子化レンジ１２１はＭＳＢ－１時の量子化レンジ１２０の基準電位Ｖref１２以上のレベルを２倍したものとなり、ＭＳＢ－２の位の量子化の為のレンジ拡大処理を実現している。量子化レンジ１２１は量子化レンジ１２０に対して２倍にレンジ拡大されているので、フルレンジを２通りに分割した量子化範囲をもち、図１のコンパレーター３の基準電源の基準電位Ｖref１２は量子化レンジ１２１の中心に位置し、この値を超えた場合、図１のコンパレーター３の出力は“Ｈ”になり、ＭＳＢ－２（ＬＳＢ）の量子化コードは“１”に確定する。入力アナログ信号がこの値を超えなかった場合、コンパレーター３の出力は“Ｌ”となりＭＳＢ－２（ＬＳＢ）の量子化コードは“０”に確定する。図２の例では、入力アナログ信号１８が基準電位Ｖref１２よりも大きい為、コンパレーター３の出力は“Ｈ”となり、ＭＳＢ－２（ＬＳＢ）の“１”が確定する。これにより、ＭＳＢ，ＭＳＢ－１，ＭＳＢ－２（ＬＳＢ）と順に逐次比較され０１１のＡＤ変換コードがエンコードされる。

【００２４】この様にＡＤ変換したアナログ信号をレンジ拡大処理し、帰還巡回させ、再度ＡＤ変換することにより、シンプルな回路構成により高精度の逐次比較が可能となった。すなわち従来例で示したＤＡコンバーター５４を必要とせず、ＡＤ変換の量子化ビット数を増加させても、従来例の様に内蔵のＤＡコンバーター５４の変換精度でＡＤ変換の精度が決り高精度化が難しかったのに対し、本実施例によれば、減算処理回路７の減算精度とレンジ拡大処理の信号増幅手段２及びコンパレーター３の判定精度のみで決まる為、量子化ビット数を上げてもＡＤ変換の量子化誤差の増加にはつながらず、多ビットの高精度な逐次比較型ＡＤコンバーターを可能とした。

［第２の実施例］図３は、本発明の第２の実施例を示す回路図である。図３において、入力端子１に、ＡＤ変換されるアナログ信号が印加され、スイッチ手段８に入力される。スイッチ手段８の他方の入力は第二のサンプルホールド回路６に接続されており、ＭＳＢ以降のアナログ変換信号が保持されている。スイッチ手段８の出力はスイッチ手段２０に入力され、スイッチ手段２０の他方の入力は、接地電位２７に接続されている。スイッチ手段２０の出力は第一の容量手段２３に接続され、第一の容量手段２３の他方の端子は、演算増幅器２の非反転入力端子（＋入力端子）に接続される。演算増幅器２の反転入力端子（－入力端子）には、第二の容量手段２４と第三の容量手段２５が共通接続されており、第三の容量手段２５の他方の端子は演算増幅器２の出力に接続され、容量結合の帰還ループを形成する。第二の容量手段２４の他方の端子はスイッチ手段９の出力が接続され、スイッチ手段９の一方の入力端子は基準電源１２に接続され、他方の入力端子は接地電位２７に接続されている。又スイッチ手段９の制御端子はコンパレーター３の出力でコントロールされ、ここで信号減算処理が行われる。また演算増幅器２の出力はスイッチ手段２２を通して演算増幅器２の反転入力端子に接続され、リセット制御信号２６をアクティブにすることで、演算増幅器２をゲイン１のボルテージフォロアのモードにセットする。演算増幅器２の非反転入力端子と第一の容量手段２３の共通接続点にはスイッチ手段２１を通して、接地電位２７に接続されており、リセット制御信号２８でオンし、演算増幅器２の非反転入力端子を接地電位２７にリセットする。演算増幅器２の出力は、コンパレーター３の非反転入力端子とスイッチ手段１１に接続されており、コンパレーター３の反転入力端子には、基準電源の基準電圧Ｖref１２が印加され、演算増幅器２の出力が基準電位Ｖref１２より大きい場合は“Ｈ”を出力し、小さい場合は“Ｌ”を出力する。このコンパレーター３の出力

が逐次比較されている入力アナログ信号の量子化出力であり、かつスイッチ手段９の制御信号となり、ＡＤ変換後の入力アナログ信号の後処理（減算処理か、何もしないか）を制御している。ＡＤ変換後の入力アナログ信号の後処理された信号は、スイッチ手段１１を通して第一のサンプルホールド回路５に入力され、次桁のＡＤ変換用アナログ信号として、保持される。保持された信号はスイッチ手段１３を通して第二のサンプルホールド回路６に入力され、第二のサンプルホールド回路６の出力からＭＳＢ以降のＡＤ変換用アナログ信号Ｖinがスイッチ手段８を通して入力部に巡回帰還される。

【００２５】以後、各モードにおける動作を図面を用いて説明する。図４～図７を用いてＭＳＢ変換時の回路動作を説明する。図３において、スイッチ手段８を入力端子１側に倒し、最初にＡＤ変換するアナログ信号をスイッチ手段２０の入力端子に印加する。この時の等価回路を図４に示す。

【００２６】演算動作に入る前に必ずリセットモードを持ち各容量手段の初期値を設定する。スイッチ手段２０は接地電位２７に接続され、スイッチ手段２１はオンし接地電位２７に接続され、スイッチ手段２２はオンし演算増幅器２の出力と反転入力端子をショートし演算増幅器２をボルテージフォロアのモードに固定する。スイッチ手段９は接地電位２７に接続される。図５はＭＳＢ変換リセット時の等価回路図である。第一の容量手段２３の両端は接地電位２７に接続され、演算増幅器２の反転入力端子は、出力とショートされボルテージフォロアとなっており、演算増幅器２の非反転入力端子は接地電位２７に接続されている為、演算増幅器２の出力も接地電位２７と同電位となる。

【００２７】次にスイッチ手段２０を入力端子１側に倒し、入力アナログ信号を取り込み量子化処理する。この信号入力比較モードを図６に示す。第一の容量手段２３の片側には入力端子１が接続され、端子の電位は接地電位から入力されたアナログ信号に変化する。容量手段２３の他方の端子に接続されているスイッチ手段２１はオフとなるので、演算増幅器２の非反転入力端子は高インピーダンスであるのでこのポイントはフローティングとなり、第一の容量手段２３の入力端子の電位の変化分と同じだけ変化する為、演算増幅器２の出力はVinと等しくなる。コンパレーター３はこのVinを受け、入力アナログフルレンジの１／２の電圧である基準電源の基準電圧Vref１２と比較され、Vinが基準電圧Vref１２よりも大きい場合“Ｈ”を出力しＭＳＢの量子化コードを“１”に確定し、Vinが基準電圧Vref１２よりも小さい場合“Ｌ”を出力しＭＳＢの量子化コードを“０”に確定し、出力端子４に出す。

【００２８】回路はここでＭＳＢ変換動作を終えＭＳＢ－１変換の為の前処理及びレンジ拡大処理に移行する。図７に後処理及びレンジ拡大処理モードの等価回路図を示す。コンパレーター３の出力４はスイッチ手段９の制御端子に接続されており、Vinが基準電圧Vref１２よりも小さい場合、スイッチ手段９の制御端子には“Ｌ”が入力され、接地電位２７に接続されたままの状態となる。この時、スイッチ手段２２はオフし演算増幅器２の反転入力端子と出力の間には、第三の容量手段２５が接続された形となる。第二の容量手段２４と第三の容量手段２５の容量値は等しく設定されており、スイッチ手段２２がオフすると同時に、演算増幅器２のゲインは２倍に設定され、ＭＳＢ変換時に用いた入力アナログ信号Ｖinを２倍して出力する。この時、スイッチ手段１１は、演算増幅器２のゲインが１から２倍に推移する間はオンし、ゲインが２倍に設定されて出力が安定した時点でオフする。このサンプリング動作により第一のサンプルホールド回路５にはＭＳＢ時に比較したVinの２倍の電圧を保持することになり、次の下位ビットの量子化動作時にＡＤ変換部のアナログ入力端子に巡回帰還させる。Ｖinが基準電源の基準電圧Vref１２よりも大きい場合、スイッチ手段９の制御端子には“Ｈ”が入力され、スイッチ手段９は入力を接地電位２７から基準電圧Vref１２に切り替える。この時点でスイッチ手段２２はオフし演算増幅器２の反転入力端子と出力の間には、第三の容量手段２５が接続された形となる。第二の容量手段２４と第三容量手段２５の容量値は等しく設定されており、スイッチ手段２２がオフすると同時に、スイッチ手段９も接地電位２７から基準電圧Vref１２に推移する為、VinからVrefを引いたVin－Vrefを演算増幅器２が２倍して出力する。この時、スイッチ手段１１は、演算増幅器２のフローティングポイントがVin－Vref演算を行い、ゲインが１から２倍に推移する間はオンし、ゲインが２倍に設定されて出力が安定した時点でオフする。このサンプリング動作により第一のサンプルホールド回路５にはＭＳＢ時に比較したVinからVrefを引いた電圧の２倍の値を保持することになり、次の下位ビットの量子化動作時にＡＤ変換部のアナログ入力端子に巡回帰還させる。

【００２９】以上、図４～図７で説明した通り、容量結合型演算増幅器を用いてＭＳＢ変換後、処理ゲイン１で信号増幅された入力アナログ信号はコンパレーター３により基準電圧Vref１２と比較され量子化されると共に、次の桁ＭＳＢ－１の処理為、入力アナログ信号を後処理（量子化コードが“０”の時、何もせず、量子化コードが“１”の時、Vin－Vrefの減算処理を行う。）及びレンジ拡大処理（後処理後のアナログ信号を２倍して、ＡＤ変換される次の桁ＭＳＢ－１のスケールに合わせる。）をしサンプルホールド回路を通して入力に巡回帰還させる。

【００３０】ＭＳＢ以降特にＭＳＢ－１ビットのＡＤ変換のアーキテクチャーを、図８～図１１を用いて説明する。

【００３１】図８に、ＭＳＢ－１のＡＤ変換時の等価回路を示す。スイッチ手段８を、後処理及びレンジ拡大処理が施されたＭＳＢ－１桁用アナログ信号電圧が保持されている第二のサンプルホールド回路６の出力側に倒し、この信号を次のＡＤ変換用アナログ信号として入力する。またスイッチ手段１３をオフにして第二のサンプルホールド回路６には、ＭＳＢ－１桁用アナログ信号電圧を保持した状態を保つ。

【００３２】演算動作に入る前に必ずリセットモードを持ち各容量手段の初期値を設定する。スイッチ手段２０は接地電位２７に接続され、スイッチ手段２１はオンし接地電位２７に接続され、スイッチ手段２２はオンし演算増幅器２の出力と反転入力端子をショートし演算増幅器２をボルテージフォロアのモードに固定する。スイッチ手段９は接地電位２７に接続される。図９はＭＳＢ－１変換リセット時の等価回路図である。第一の容量手段２３の両端は接地電位２７に接続され、演算増幅器２の反転入力端子は、出力とショートされボルテージフォロアとなっており、演算増幅器２の非反転入力端子は接地電位２７に接続されている為、演算増幅器２の出力も接地電位２７と同電位となる。

【００３３】次にスイッチ手段２０をスイッチ手段８側（第二のサンプルホールド回路６の出力側）に倒し、ＭＳＢ－１桁用アナログ信号電圧を取り込み量子化処理する。このＭＳＢ－１桁用アナログ信号入力比較モードを図１０に示す。第一の容量手段２３の片側には第二のサンプルホールド回路６の出力が接続され、端子の電位は接地電位から入力されたＭＳＢ－１桁用アナログ信号電圧２９に変化する。容量手段２３の他方の端子に接続されているスイッチ手段２１はオフとなるので、演算増幅器２の非反転入力端子は高インピーダンスであるのでこのポイントはフローティングとなり、第一の容量手段２３の入力端子の電位の変化分と同じだけ変化する為、演算増幅器２の出力はＭＳＢ－１桁用アナログ信号電圧２９と等しくなる。コンパレーター３はこのＭＳＢ－１桁用アナログ信号電圧を受け、入力アナログフルレンジの１／２の電圧である基準電圧Ｖref１２と比較され、ＭＳＢ－１桁用アナログ信号電圧が基準電圧Ｖref１２よりも大きい場合“Ｈ”を出力しＭＳＢ－１の量子化コードを“１”に確定し、ＭＳＢ－１桁用アナログ信号電圧が基準電圧Ｖref１２よりも小さい場合“Ｌ”を出力しＭＳＢ－１の量子化コードを“０”に確定し、出力端子４に出す。

【００３４】回路はここでＭＳＢ－１桁変換動作を終えＭＳＢ－２桁変換の為、ＭＳＢ－１桁アナログ信号の後処理及びレンジ拡大処理に移行する。図１１に前処理及びレンジ拡大処理モードの等価回路図を示す。コンパレーター３の出力端子４はスイッチ手段９の制御端子に接続されており、ＭＳＢ－１桁用アナログ信号電圧が基準電圧Ｖref１２よりも小さい場合、スイッチ手段９の制御端子には“Ｌ”が入力され、接地電位２７に接続されたままの状態となる。この時、スイッチ手段２２はオフし演算増幅器２の反転入力端子と出力の間には、第三の容量手段２５が接続された形となる。第二の容量手段２４と第三の容量手段２５の容量値は等しく設定されており、スイッチ手段２２がオフすると同時に、演算増幅器２のゲインは２倍に設定され、ＭＳＢ－１変換時に用いたＭＳＢ－１桁用アナログ信号電圧を２倍して出力する。この時、スイッチ手段１１は、演算増幅器２のゲインが１から２倍に推移する間はオンし、ゲインが２倍に設定されて出力が安定した時点でオフする。このサンプリング動作により第一のサンプルホールド回路５にはＭＳＢ－１時に比較したＭＳＢ－１桁用アナログ信号電圧の２倍の電圧を保持することになり、次の下位ビットＭＳＢ－２の量子化動作時にＡＤ変換部のアナログ入力端子に巡回帰還させる為、第一のサンプルホールド回路５に保持されているＭＳＢ－１桁用アナログ信号電圧をスイッチ手段１３をオンにして第二のサンプルホールド回路６に転送する。ＭＳＢ－１桁用アナログ信号電圧が基準電圧Ｖref１２よりも大きい場合、スイッチ手段９の制御端子には“Ｈ”が入力され、スイッチ手段９は入力を接地電位２７から基準電圧Ｖref１２に切り替える。この時点でスイッチ手段２２はオフし演算増幅器２の反転入力端子と出力の間には、第三の容量手段２５が接続された形となる。第二の容量手段２４と第三の容量手段２５の容量値は等しく設定されており、スイッチ手段２２がオフすると同時に、スイッチ手段９も接地電位２７から基準電圧Ｖref１２に推移する為、ＭＳＢ－１桁用アナログ信号電圧からＶrefを引いた、（ＭＳＢ－１桁用アナログ信号電圧）－Ｖrefを演算増幅器２が２倍して出力する。この時、スイッチ手段１１は、演算増幅器２のフローティングポイントが（ＭＳＢ－１桁用アナログ信号電圧）－Ｖref演算を行い、ゲイン１から２倍に推移する間はオンし、ゲインが２倍に設定されて出力が安定した時点でオフする。このサンプリング動作により第一のサンプルホールド回路５にはＭＳＢ－１時に比較したＭＳＢ－１桁用アナログ信号電圧からＶrefを引いた電圧の２倍の値を保持することになり、次の下位ビットＭＳＢ－２の量子化動作時にＡＤ変換部のアナログ入力端子に巡回帰還させる為、第一のサンプルホールド回路５に保持されているＭＳＢ－１桁用アナログ信号電圧をスイッチ手段１３をオンにしてサンプルホールド回路６に転送する。

【００３５】以上、図８～図１１で説明した通り、容量結合型演算増幅器を用いてＭＳＢ－１桁のＡＤ変換時、処理ゲイン１で信号増幅された入力アナログ信号はコンパレーター３により基準電圧Ｖref１２と比較され量子化されると共に、次の桁ＭＳＢ－２の処理為、ＭＳＢ－１桁用アナログ信号電圧を後処理（量子化コードが“０”の時、何もせず、量子化コードが“１”の時、Ｍ

ＳＢ－１桁用アナログ信号電圧－Ｖrefの減算処理を行う。）及びレンジ拡大処理（後処理後のアナログ信号を２倍して、ＡＤ変換される次の桁ＭＳＢ－２のスケールに合わせる。）をしサンプルホールド回路を通して入力に巡回帰還させる。

【００３６】この様にＡＤ変換したアナログ信号をレンジ拡大処理し、巡回帰還させ、再度ＡＤ変換することにより、シンプルな回路構成により高精度の逐次比較が可能となった。すなわち従来例で示したＤＡコンバーター５４を必要とせず、ＡＤ変換の量子化ビット数を増加させても、従来例の様に内蔵のＤＡコンバーター５４の変換精度でＡＤ変換の精度が決り高精度化が難しかったのに対し、本実施例によれば、容量結合型演算増幅器の演算精度及びコンパレーターの判定精度のみで決まる為、量子化ビット数を上げてもＡＤ変換の量子化誤差の増加にはつながらず、多ビットの高精度な逐次比較型ＡＤコンバーターを可能とした。また、従来例の逐次比較型ＡＤコンバーターでは、量子化ビット数を増加すると内蔵されるＤＡコンバーター５４のビット数もＮビット化しなければならず、回路規模が増加したが、本実施例による回路では量子化ビット数をあげても回路の増加はなく、高集積度、低消費電力の逐次比較型ＡＤコンバーターを可能とした。

【００３７】

【発明の効果】以上説明したように、本発明によれば、ＭＳＢより逐次変換するＡＤコンバーターにおいて、信号増幅手段とサンプルホールド回路を用いてＡＤ変換したアナログ信号を、その桁の量子化結果に基ずき減算処理やレンジ拡大処理を実行して、次桁の処理可能なアナログ電圧に変換してから、入力に帰還し次桁のＡＤ変換を行う処理を単一のハードウェアで実現したことにより、シンプルな回路構成により高精度の逐次比較ＡＤ変換動作が可能となった。また量子化ビット数を増加してもハードウェアの増加が無いフレキシブルな回路を採用したことで、高集積度、低消費電力の逐次比較型ＡＤコンバーターを可能とした。

【図面の簡単な説明】

【図１】本発明の第一実施例を示す回路図である。

【図２】第一実施例のアーキテクチャーの説明図である。

【図３】本発明の第二実施例を示す回路図である。

【図４】第二実施例のＭＳＢ変換時の動作を説明する回路図である。

【図５】第二実施例のＭＳＢ変換時の動作を説明する回路図である。

【図６】第二実施例のＭＳＢ変換時の動作を説明する回路図である。

【図７】第二実施例のＭＳＢ変換時の動作を説明する回路図である。

【図８】第二実施例のＭＳＢ以降のビットのＡＤ変換の動作を説明する回路図である。

【図９】第二実施例のＭＳＢ以降のビットのＡＤ変換の動作を説明する回路図である。

【図１０】第二実施例のＭＳＢ以降のビットのＡＤ変換の動作を説明する回路図である。

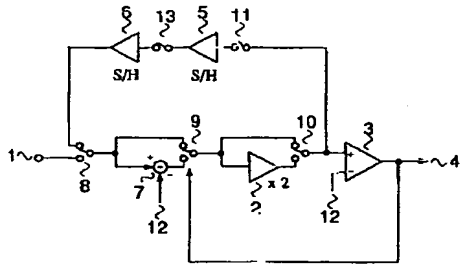
【図１１】第二実施例のＭＳＢ以降のビットのＡＤ変換の動作を説明する回路図である。

【図１２】従来の逐次比較型ＡＤコンバーターの回路図である。

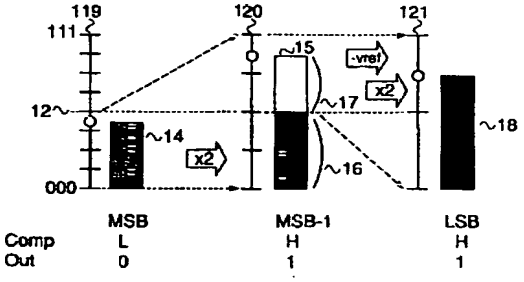
【符号の説明】

１　入力端子
２　信号増幅手段
３　コンパレーター
４　出力端子
５　第一のサンプルホールド回路
６　第二のサンプルホールド回路
７　減算処理回路
８　スイッチ手段
９　スイッチ手段
１０　スイッチ手段
１１　スイッチ手段
１２　基準電圧Vref
１３　スイッチ手段
１４　アナログ信号
１５　アナログ信号
１６　アナログ信号
１７　アナログ信号
１８　アナログ信号
１１９　量子化レンジ
１２０　量子化レンジ
１２１　量子化レンジ
２０　スイッチ手段
２１　スイッチ手段
２２　スイッチ手段
２３　第一の容量手段
２４　第二の容量手段
２５　第三の容量手段
２６　リセット信号
２７　接地電位
２８　リセット信号
２９　ＭＳＢ－１桁用アナログ信号電圧
５０　入力端子
５１　コンパレーター
５２　制御回路
５３　比較制御レジスタ
５４　ＤＡコンバーター

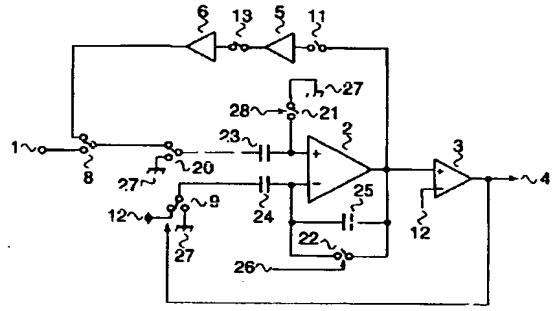
【図1】



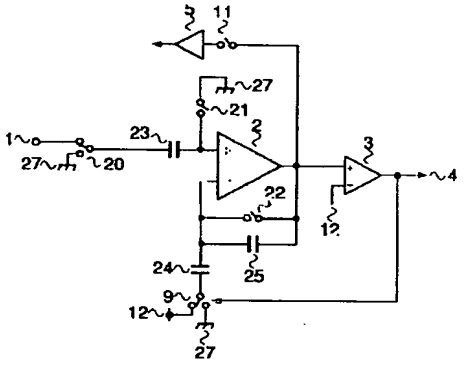
【図2】



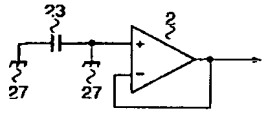
【図3】



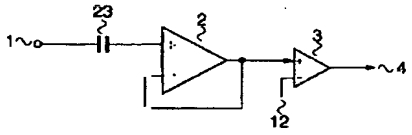
【図4】



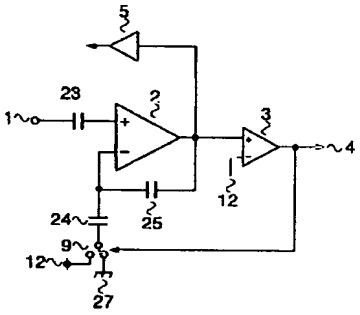
【図5】



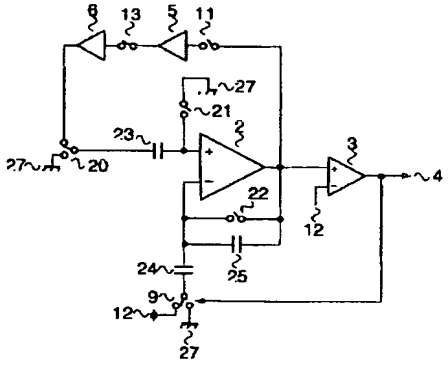
【図6】



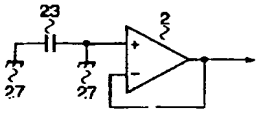
【図7】



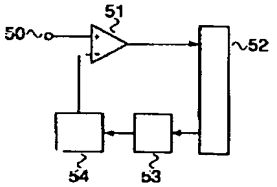
【図8】



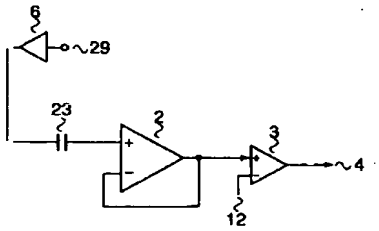
【図9】



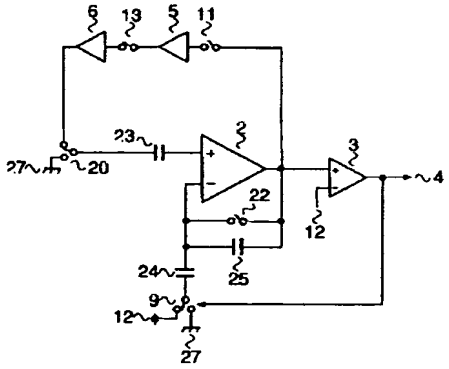
【図12】



【図１０】



【図１１】



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